Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OFFSET NULL N1**
2. **– INPUT**
3. **+ INPUT**
4. **VCC –**
5. **OFFSET NULL N2**
6. **OUTPUT**
7. **VCC +**
8. **NC**

**.060”**

**8**

**4 5**

**7**

**6**

**1**

**2**

**3**

**MASK**

**REF**

**TL061B**

**.040”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC**

**Mask Ref: TL061B**

**APPROVED BY: DK DIE SIZE .040” X .060” DATE: 4/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .016” P/N: TL061**

**DG 10.1.2**

#### Rev B, 7/1